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2002 J. Phys.: Condens. Matter 14 13403

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J. Phys.: Condens. Matter **14** (2002) 13403–13410 PII: S0953-8984(02)54245-4

Crystal defects and junction properties in the evolution of device fabrication technology

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Received 3 October 2002
Published 22 November 2002
Online at stacks.iop.org/JPhysCM/14/13403

Abstract
In this paper, the correlation between dislocation density and transistor leakage current is demonstrated. The stress evolution and the generation of defects are studied as a function of the process step, and experimental evidence is given of the role of structure geometry in determining the stress level and hence defect formation. Finally, the role of high-dose implantations and the related silicon amorphization and recrystallization is investigated.

1. Introduction

It is usually recognized that metal-decorated defects in the space-charge region of the junction are the most harmful, in that they can be responsible for an anomalous increase of the electric field resulting in a 'soft' junction reverse characteristic [1] or a decreased breakdown voltage. However, as the device size shrinks, the electrical activity of the defects changes. The excess junction reverse current is reduced, but another junction failure is observed in association with crystal defectivity, consisting of a source-to-drain leakage of transistors due to pipeline defects. Pipeline defects have been widely reported in bipolar devices [2] and recently also in complementary-metal–oxide–semiconductor (CMOS) technology [3, 4]. This failure is explained by an anomalous dopant diffusion along the defect, making the defect act as a resistive path. On the other hand, the dopant diffusing along the defects includes most of those in the neutral region of the junction, thus limiting the efficiency of the defects in increasing junction reverse current.

Defect formation is very often related to isolation technology, which is responsible for the development of a significant stress in silicon and hence for the generation and growth of dislocations. This effect becomes more and more important with shrinking device size and it is dramatic when shallow-trench-isolation (STI) technology is used [5, 6]. In addition, high-dose implantations are known to play an important role in defect generation [7]. The defect formation mechanism may involve both the recrystallization of the amorphous layer and the

0953-8984/02/4813403+08$30.00 © 2002 IOP Publishing Ltd Printed in the UK

residual point defect excess. In a previous study, dislocation formation was found to be related to the amorphous layer depth [8].

In this paper, the correlation between dislocation density and transistor leakage current is demonstrated. The stress evolution and the generation of defects are studied as a function of the process step, and experimental evidence is given of the role of structure geometry in determining the stress level and hence defect formation. Finally, the role of high-dose implantations and the related silicon amorphization and recrystallization is investigated.

2. Experimental details

2.1. Sample preparation

This work is based on a 0.18 μm CMOS technology with STI. An array of two thousand transistors was used as a monitor vehicle. The active-area geometry of transistors was designed to maximize the probability of the formation of dislocations [9]. As will be shown later, this can be achieved by increasing the number of corners in the active-area pattern and by reducing the active-area-to-active-area spacing (0.28 μm). The transistors have a 0.28 μm channel width and a 0.18 μm channel length.

The process flow of a 0.18 μm non-volatile memory was used for the fabrication of the monitor structures. The active-area pattern is defined and is etched to create trenches of 3500 Å. The trenches are filled by oxide deposition and annealed before chemical mechanical polishing (CMP). After the well implantations and the active oxide growth, the gate stack is defined. Light-doping drain (LDD) implantations of As and B are followed by Si_3N_4 spacer formation and high-dose As and B source/drain implantations for n- and p-channel transistors, respectively. The implantation damage is annealed by a rapid thermal process (RTP). The silicide formation and back-end process flow concludes the process.

The mechanical stress evolution and dislocation formation were monitored at different process steps.

2.2. Techniques

Transistor arrays were electrically tested by measuring the drain current under subthreshold conditions (0 V gate and source bias, −1.8 V substrate bias and 1.8 V drain bias). We define this measurement as the 'channel leakage current' measurement. In non-defective structure this current consists of the subthreshold current only (about 10^{-7} A or less). Defects have a typical electrical signature, in that they are responsible for increases of the channel leakage current by various orders of magnitude, with a roughly resistive current–voltage characteristic. In addition, in defective structures the channel leakage current is approximately independent of the substrate and gate voltages.

The elastic stress in silicon was evaluated by means of Raman [10] shift measurements and the convergent beam electron diffraction (CBED) [11, 12] technique using transmission electron microscopy (TEM). Raman shift measurements require specific structures because of the limited spatial resolution of this technique. For this reason, 3 μm wide, 2 μm spaced active-area stripes were used for these measurements.

TEM was also used for the identification of crystal defects. However, no statistical information can be obtained by TEM analyses, because TEM can analyse very limited silicon volumes only. For this reason, the dislocation density was evaluated by wafer delayering, selective etching and scanning emission microscopy (SEM) inspections. Leaky points were identified by emission microscopy (EMMI) [13] of defective structures.

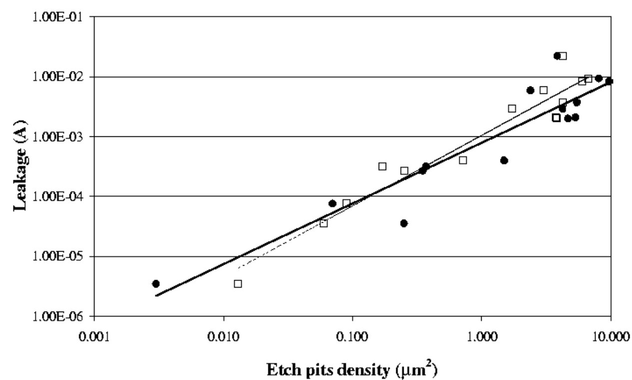

Figure 1. The channel leakage versus the etch pit densities measured both at the wafer edges (dots) and at the wafer centre (squares). The trends were obtained from both distributions and are shown in the graph (the thick line for the edge distribution, the thin one for the centre distribution). They are functions proportional to x^{α}, where α is almost 1.

3. Results

3.1. Electrical versus crystal defects

In order to demonstrate the link between dislocations and channel leakage, EMMI-characterized leaky structures were inspected after Secco etching. Dislocation etch pits were always found at the location of the emission points. However, no one-to-one correspondence between etch pits and emission points could be established, because dislocations can be electrically inactive depending on their location and on dopant decoration.

For this reason, a statistical correlation was established between the measured channel leakage and Secco etch pits by a systematic inspection of electrically tested structures.

Figure 1 reports the measured channel leakage versus the etch pit density. The etch pit densities were measured both at the wafer edges (dots) and at the wafer centre (squares). In both regions of the wafers a very good correlation is obtained, with the channel leakage increasing approximately in proportion to the etch pit density. So it is possible to conclude that most of the etch pits are electrically active dislocations.

3.2. Step-by-step analysis of the process flow

A step-by-step analysis of the process flow was carried out in order to identify the process steps responsible for elastic stress increase and the process steps where defects are generated. Raman shift measurements and SEM inspections after Secco etching were carried out on samples at various process levels. Specifically, wafers were inspected after the gate oxidation of the high-voltage transistor, after the oxidation of the gate electrode polysilicon, after the LDD implantation annealing and, finally, after high-dose implantation annealing. In order to discriminate between radiation damage and stress accumulation effects, an additional wafer that did not undergo the high-dose implantation, receiving only the annealing, was also analysed. The SEM inspection after delayering and selective etching showed no defects up to the LDD implantations. Very few crystal defects appear after LDD implantation annealing, but it is after the high-dose implantation annealing that the significant growth in the dislocation density occurred. In addition, this defect growth was not observed in the sample that had not undergone the high-dose implantation. The results of this analysis confirmed that the critical step for dislocation formation in a CMOS process is the high-dose implantation.

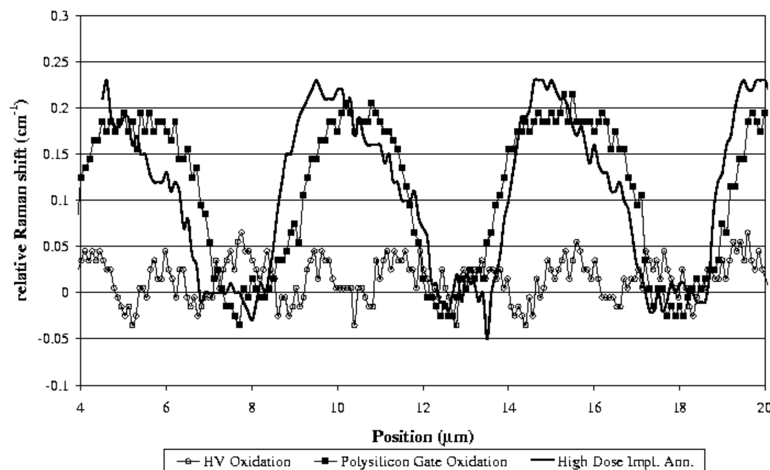

Figure 2. The micro-Raman measurements of the most relevant samples in the step-by-step analysis. To obtain an estimate of the stress magnitude, we assume that silicon is under uniaxial stress along x, where x is the direction perpendicular to the active-area stripes. Under this assumption, the relationship between the Raman shift and stress is: σ_{xx} (MPa) $= -500\,\Delta\omega\,(\mathrm{cm}^{-1})$.

As the formation of defects alters the stress distribution, stress measurements are not significant in samples where defects are formed, and for this reason no stress measurements were carried out on high-dose-implanted samples. Apart from this exception, the analysis of the stress evolution during the process was carried out according to the same scheme as the crystal defectivity analysis.

The Raman shift measurements (figure 2) showed that mechanical stress is very low up to the gate oxidation of the high-voltage transistor. After the oxidation of the polysilicon gate electrode, the stress level reaches a maximum and it is not significantly changed in subsequent process steps. So the step-by-step analysis shows that a relevant mechanical stress level in silicon is reached by subsequent oxidations of the STI structure; however, this stress level is sustained without dislocation formation until the high-dose implantations occur.

3.3. The role of mechanical stress

Too high a mechanical stress is very well known [14] to cause defect formation. Our data show that in silicon processing, other factors enhance this phenomenon.

Experimentally we observe that defect formation strongly depends on active-area geometry. Specifically, a reduced active-area size and spacing and a high density of corners make a structure prone to defect generation. As an example of this, figure 3 shows the SEM images of two different geometries from the same sample after delayering and Secco etching. It is immediately seen that the structure with the highest corner density also exhibits the largest dislocation density at the end of the process. Three-dimensional calculations of the stress in silicon [15] show that the active-area corners are maximum stress points, so the observed geometrical dependence of defect generation can be explained in terms of mechanical stress.

Further and more persuasive evidence of the stress role is provided by the comparison between two processes with different mechanical stress levels. The strain in silicon was measured by Raman shift measurements and by the CBED technique before LDD implantation (the last step before dislocation generation). Figure 4 shows the micro-Raman results and

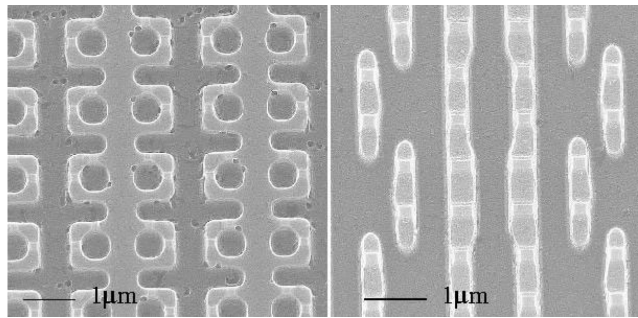

Figure 3. The SEM images of two different geometries after delayering and selective etching. The structure with the highest corner density also exhibits the largest dislocation density.

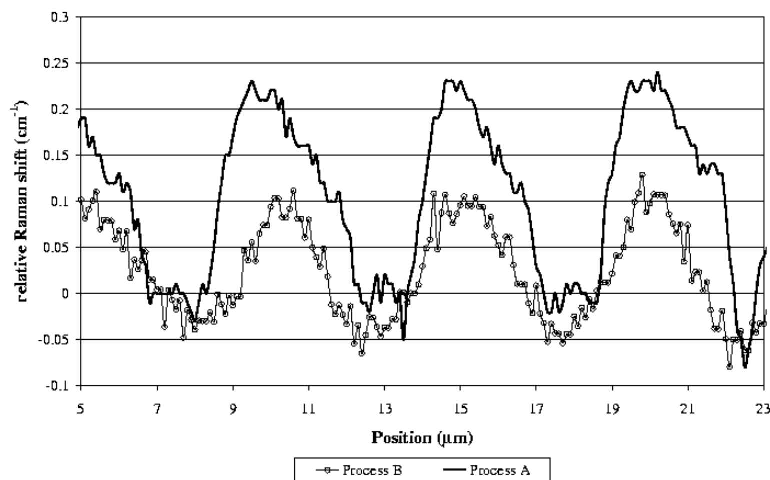

Figure 4. The micro-Raman measurements for two different processes.

figure 5 the CBED strain maps for the two processes. The micro-Raman and CBED techniques consistently show that process A induces a higher strain level in silicon than process B. Some wafers from the same lots as the samples in figures 4 and 5 were electrically tested at the end of the process. The electrical results (figure 6) show that the channel leakage in the monitor structure decreases in the process with the lower stress level (B). Also a crystallographic analysis confirms that the etch pit density is much lower in the B process than in the A process wafers.

Using the CBED measurements it is possible to map the strain field across the active area. So the previous CBED data (figure 5(b)) show that at the top corner of the active area the stress is maximum and compressive. In the centre there is a tensile stress zone. At the bottom there is a compressive stress zone and the measured value is about one order of magnitude lower than that at the top and of the order of the technique sensitivity. So it is clear that the most critical zone is the top corner of the active area.

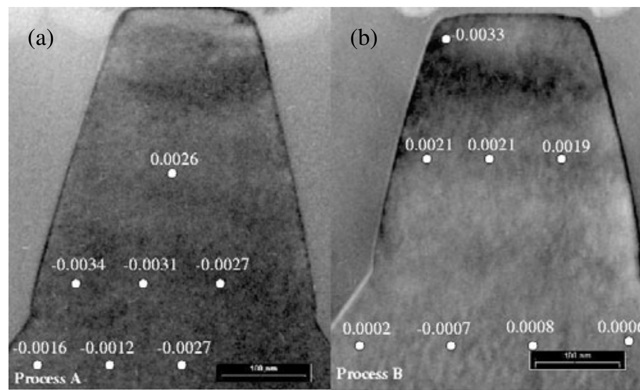

Figure 5. The CBED strain map of the active-area cross-section for two different processes. At the top of the cross-section of process A the stress is very high. As a consequence, the stress gradient is too large for the measurement.

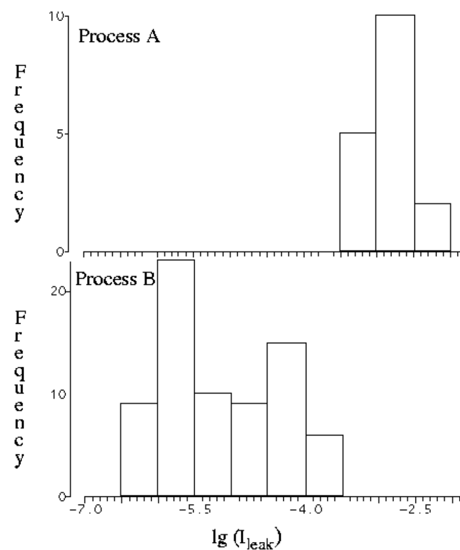

Figure 6. The channel leakage in the monitor structure for the two different processes in figures 4 and 5. The channel leakage decreases in the process with the lower stress level (B).

3.4. The role of high-dose implantation

Both crystal defects and the channel leakage problem appear in the n-channel (arsenic-implanted) regions only; no such phenomenon is observed in p-channel (boron-implanted) regions. As the arsenic implantation produces an amorphous layer and the boron implantation does not, this result suggests that the formation and recrystallization of the amorphous layer are critical for defect formation.

It was previously shown that the energy of the high-dose arsenic implantation affects the dislocation formation and the magnitude of the channel leakage [8]. This fact was also confirmed in this study and suggests a role of the extent of the amorphous layer in defect formation.

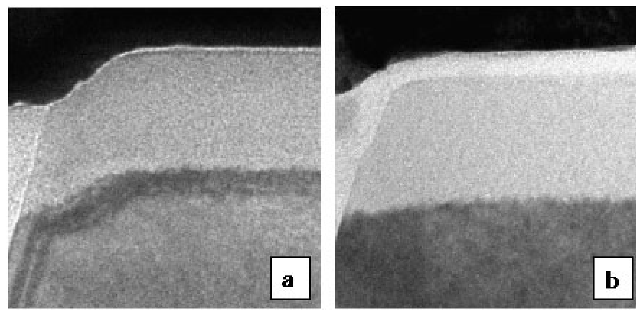

Figure 7. The TEM cross-section of the monitor structure after high-dose implantation. The amorphous zone is visible.

Finally, we observed that the amorphous layer morphology can be affected by significant two-dimensional effects which strongly depend on implantation conditions. Figure 7 shows the TEM cross-section of as-implanted samples obtained by different implantation processes. In regions far enough from the active-area edge, the samples have roughly the same amorphous layer depth. In contrast, in the region close to the active-area edge the extension of the amorphous layer is significantly larger in the figure 7(a) sample than in the 7(b) sample. It was found that processes that reduce the amorphous layer width in the top corner of the active area (see figure 7(b)) strongly reduce both the transistor channel leakage and the defect density as observed by selective etching and SEM inspection.

4. Discussion and conclusions

The previous results suggest that the critical factors for pipeline defect formation are the mechanical stress level just before the high-dose implantation and the high-dose implantation process. As regards mechanical stress, both experimental results and numerical calculations show that the most stressed zones are found in the top corner of the active area. As regards high-dose implantations, both the related point defect excess and the amorphization–recrystallization process could be involved in defect formation. However, no defects are found in boron-implanted regions. High-dose boron implantations produce a large point defect excess, though they do not create any amorphous layer at least in room temperature implantation processes [16]. We can therefore conclude that in our process the high-dose implantations contribute to extended defect generation through the amorphization and recrystallization of the implanted region. In the previous section we gave evidence that the amorphous layer width is critical for defect formation—and more specifically the extent of the amorphous layer in the highly stressed region. We suggest that in the recrystallization of a highly stressed region, defect formation may be energetically preferred over the regrowth of a strained perfect crystal.

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